

**AMENDMENTS TO THE CLAIMS**

1-2. (Cancelled)

3. (Currently Amended) A noise eliminating system on chip, comprising:

a chip having two guiding devices; and

at least one noise eliminating system built ~~in~~ on a surface of the chip;

wherein the noise eliminating system has two terminals ~~which are being~~ electrically connected to the two guiding devices respectively ~~on the upper layer of the chip and are being~~ electrically connected to a power supply unit and a grounding unit of the chip respectively.

4. (Currently Amended) A noise eliminating system on chip, comprising:

a chip; and

at least one noise eliminating system built ~~in~~ on a surface of the chip;

a guiding unit including two guiding devices, the guiding unit being on the surface of the chip, the two guiding devices being electrically connected to a power supply and a ground respectively;

wherein the two terminals of the noise eliminating system are electrically connected to the power supply and the ground respectively ~~an additional~~ via the two guiding device devices on the chip and are connected to respective power supply and grounding.

5. (Currently Amended) The noise eliminating system on chip as claimed in claim 4 wherein the ~~additional guiding device-unit~~ on the chip is a metal redistribution layer.

6. (New) The noise eliminating system on chip of claim 3, wherein each of the two guiding devices is formed through etching a conductive material sputtered on the surface of the chip.

7. (New) The noise eliminating system on chip of claim 4, wherein each of the two guiding devices is formed through etching a conductive material sputtered on the surface of the chip.

8. (New) The noise eliminating system on chip of claim 3, wherein the noise eliminating system is a de-coupling capacitor.

9. (New) The noise eliminating system on chip of claim 4, wherein the noise eliminating system is a de-coupling capacitor.